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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,645	08/22/2003	Chandra Mouli	M4065.0674/P674	8786

24998 7590 04/23/2007

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,645	MOULI, CHANDRA	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 11, 14-20, and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,117,702 to Nakamura et al. (Nakamura) in view of U.S. Pat. No. 6,232,626 to Rhodes.

Regarding claim 1, Nakamura discloses a pixel cell for an image sensor, the pixel comprising: a a photodiode (Figure 5) for generating charge in response to light and for amplifying the generated charge, the photodiode being over a surface of the substrate and comprising at least two of a first layer (25a), having a first band gap and at least two of a second layer (25b) having a second band gap, where the first layers are alternated with the second layers. Nakamura discloses use of the photodiode in an image sensor (col 1 lines 12-18). Nakamura fails to explicitly disclose a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode. Rhodes discloses a photodiode with a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura to include the gate of a transistor as in Rhodes in order to process the results of the photo detection.

Regarding claims 2 and 3, Nakamura discloses the differences of the conduction band energies of the first layer and the second layer layers as greater than a difference between the valance band energies of the first and second layer (Figure 6).

Regarding claims 4 and 20, Nakamura in view of Rhodes discloses the device of claim 1 and also discloses promoting ionization of a first carrier type and suppressing ionizing of a second carrier type (col 2 lines 6-14).

Regarding claim 11, Nakamura as modified by Rhodes further discloses the pixel cell of claim 1 where at least a portion (under light area 12) of the photodiode (24) is at a level below a level of a top surface of the substrate.

Regarding claim 14, Nakamura further discloses the used of a graded buffer layer (23/24).between a bottom layer of the photodiode and the surface of the substrate.

Regarding claim 15, Nakamura as modified by Rhodes discloses the pixel cell of claim 1, where there is a reset transistor (31) for resetting the photodiode to a predetermined voltage.

Regarding claim 16, Nakamura as modified by Rhodes discloses the pixel cell of claim 1, further comprising a floating diffusion region (30), where the transistor (28) is a transfer transistor for transferring charge from the photodiode to the floating diffusion region (col 3 lines 24-27).

Regarding claim 17, Nakamura as modified by Rhodes discloses the pixel cell of claim 1 where the photodiode is part of a CMOS image sensor (col 2 lines 44-49).

Regarding claim 18, Nakamura as modified discloses the pixel cell of claim 1 where the photodiode is part of a charge coupled device image sensor (col 1 lines 21-22).

Regarding claim 19, Nakamura as modified by Rhodes discloses the pixel cell of claim 1 where the substrate is a silicon-on-insulator substrate (Rhodes, col 6 lines 46-50).

Regarding claim 28, Nakamura as modified by Rhodes discloses the image sensor cell of claim 20, where there is a reset transistor (31) for resetting the photodiode to a predetermined voltage.

Regarding claim 29, Nakamura as modified by Rhodes discloses the image sensor of claim 20, further comprising a floating diffusion region (30), where the transistor (28) is a transfer transistor for transferring charge from the photodiode to the floating diffusion region (col 3 lines 24-27).

Regarding claim 30, Nakamura as modified by Rhodes discloses the image sensor of claim 20, where the pixel cell further comprises readout circuitry (Figure 1 transistors 36 and 38) connected (by wire 44) to a floating diffusion region (30) for reading out charge.

Regarding claim 31, Nakamura as modified by Rhodes discloses the image sensor of claim 20, further comprising circuitry (Figure 1 transistors 36 and 38) peripheral to the array, the peripheral circuitry being at a surface of the substrate, where the substrate is silicon-on-insulator (Rhodes, col 6 lines 46-50).

Claims 5-10, 12-13, 21-27 and 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,117,702 to Nakamura et al. (Nakamura) in view of U.S. Pat. No. 6,232,626 to Rhodes in view of U.S. Pat. No. 5,818,322 to Tasumi.

Regarding claims 5-6 and 21-22, Nakamura in view of Rhodes discloses the pixel cell of claim 1 and 20 as above. Nakamura in view of Rhodes fails to disclose the layers formed of a material selected from the group consisting of Si, Si_xGe_{1-x}, $Si_xGe_{1-x}C_y$, GaAs, GaAlAs, InP, InGaAs, or InGaAsP and where the first layer is Si and the second layer is SiGe. Tasumi teaches a photodiode structure (Figures 1A-1C element 2) with Si and SiGe (col 3 line 63) formed in the groove (4) of the photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rhodes to include the alternating layers of Si and SiGe as in Tasumi in order to layer improve the photodiode device performance.

Regarding claims 7-8 and 23-24, Nakamura as modified by Rhodes and Tasumi discloses where the layers of Si are doped to a first conductivity type and the layers of SiGe as taught by Tasumi are doped to a second conductivity type (col 5 lines 66-67 and col 6 lines 1-32).

Regarding claims 9-10 and 25-26, Nakamura as modified by Rhodes and Tasumi discloses the pixel cell of claim 1 where the first layer is Si_xGe_{1-x} or $Si_xGe_{1-x}C_y$ and the second layer is Si_yGe_{1-y} or $Si_xGe_yC_z$.

Regarding claim 12 and 27, Nakamura as modified by Rhodes and Tasumi discloses the photodiode comprises approximately 10 to approximately 100 layers, Tasumi has 22 layers (Figure 1A), which falls within the claimed range.

Regarding claim 13, Nakamura as modified by Rhodes and Tasumi above fails to disclose forming the layers of thickness of approximately 50 – 300 angstroms. However, one of ordinary skill in the art must balance many known factors when designing and optimizing a device. As such, varying the dimension of the thickness and would not be cause for undue experimentation. *"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) see MPEP 2144.05.* Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the thickness of the layers between 50 – 300 angstroms in order to maximize the performance of the device.

Regarding claims 32-34, Nakamura as modified by Rhodes discloses an image sensor comprising an array of pixel cells where at least one of the pixel cells comprises a photodiode (24), the photodiode comprising layers (100, 102) and a gate (28) adjacent to the photodiode for transferring the amplified charge form the photodiode.

Nakamura as modified by Rhodes fails to disclose the photodiode comprising alternating layers of Si and Si_xGe_{1-x}, where x is approximately 0.5. Tasumi teaches a photodiode structure (Figures 1A-1C element 2) with Si and Si_xGe_{1-x}, (col 3 line 63) where x is 0.6 (col 1 line 32) which is approximately 0.5 formed in the groove (4) of the photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to to include the alternating layers of Si and Si_xGe_{1-x} as in Tasumi in order to layer improve the photodiode device performance.

Regarding claims 35-37, Nakamura as modified by Rhodes discloses the image sensor of claim 20 as above. Nakamura discloses the differences of the conduction band energies of the first layer and the second layer layers as greater than a difference between the valance band energies of the first and second layer (Figure 6). Nakamura also discloses promoting ionization of a first carrier type and suppressing ionizing of a second carrier type (col 2 lines 6-14).

Nakamura as modified by Rhodes also discloses a processor system, comprising a processor (444) and an an image sensor coupled to the processor, a floating diffusion region (30) electrically connected to the first transistor and readout circuitry (Figure 1 transistors 36 and 38) electrically connected to the floating diffusion region.

Nakamura as modified by Rhodes also fails to disclose the layers formed of a material selected from the group consisting of Si, Si_xGe_{1-x}, $Si_xGe_{1-x}C_y$, GaAs, GaAlAs, InP, InGaAs, or InGaAsP and where the first layer is Si and the second layer is SiGe. Tasumi teaches a photodiode structure (Figures 1A-1C element 2) with Si and SiGe (col 3 line 63) formed in the groove (4) of the photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the alternating layers of Si and SiGe as in Tasumi in order to layer improve the photodiode device performance.

Response to Arguments

Applicant's arguments filed 02/01/2007with respect to claims 1-37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAM
4/15/2007

Sara W Crane

Sara Crane
Primary Examiner